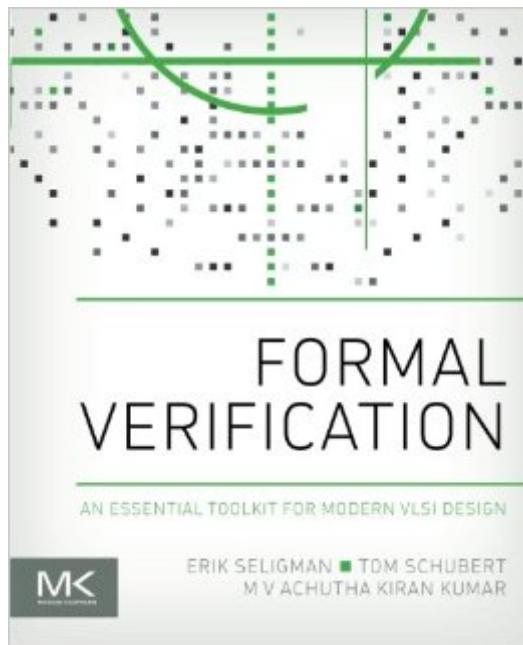


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# Formal Verification: An Essential Toolkit For Modern VLSI Design



## Synopsis

Formal Verification: An Essential Toolkit for Modern VLSI Design presents practical approaches for design and validation, with hands-on advice to help working engineers integrate these techniques into their work. Formal Verification (FV) enables a designer to directly analyze and mathematically explore the quality or other aspects of a Register Transfer Level (RTL) design without using simulations. This can reduce time spent validating designs and more quickly reach a final design for manufacturing. Building on a basic knowledge of SystemVerilog, this book demystifies FV and presents the practical applications that are bringing it into mainstream design and validation processes at Intel and other companies. After reading this book, readers will be prepared to introduce FV in their organization and effectively deploy FV techniques to increase design and validation productivity. Learn formal verification algorithms to gain full coverage without exhaustive simulation. Understand formal verification tools and how they differ from simulation tools. Create instant test benches to gain insight into how models work and find initial bugs. Learn from Intel insiders sharing their hard-won knowledge and solutions to complex design problems.

## Book Information

Paperback: 408 pages

Publisher: Morgan Kaufmann; 1 edition (August 28, 2015)

Language: English

ISBN-10: 0128007273

ISBN-13: 978-0128007273

Product Dimensions: 7.5 x 0.8 x 9.2 inches

Shipping Weight: 12.6 ounces (View shipping rates and policies)

Average Customer Review: 5.0 out of 5 stars See all reviews (3 customer reviews)

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## Customer Reviews

This book is targeted at RTL designers who want to become proficient with formal verification. It presents a staged adoption methodology starting from early design bring-up, through formal bug-hunting, to formal sign-off. In addition to traditional property checking, it also covers selected

formal "Apps" including standard protocol checking, unreachable coverage, connectivity checking, and CSR verification. There is a chapter on equivalence checking, including sequential equivalence, and a chapter on complexity management detail several advanced abstraction techniques. Though most of the focus is on practical applications, there is also a chapter giving a high level description of BDD and SAT algorithms. The discussions and examples are tool and vendor independent so this is not a replacement for tool-specific training. Many techniques are illustrated with code examples and waveforms that are complex enough to illustrate the methodology but also simple enough to follow without too much effort. The discussion starts at the beginning, assuming only knowledge of RTL design and simulation, but it progresses to advanced techniques that would benefit even expert-level readers. I have been teaching formal verification tools and techniques to industrial practitioners for many years and I believe this book is the first to focus on adoption by designers and to present such a comprehensive methodology. I will certainly be recommending it to my customers and colleagues. - Dan Benua, Formal Verification Tool Support Engineer

The subtitle of this book, "Essential Toolkit for Modern VLSI Design", has definitely met its mark, and more! This is because the authors thoroughly expressed their practical knowledge of this complex, and misunderstood topic, in an easy to read presentation. I particularly appreciated many aspects of this book, including:

1. The maturity derived from extensive years of work experiences, with successes and pitfalls.
2. The organization and presentation of the subject matters, including the progression of knowledge being presented for easier absorption of the topics.
3. The practical tips derived from actual usage of formal verification and from real designs.
4. The various approaches, or angles of attack, in using formal verification when verifying different types of designs and situations.
5. The test case examples, and progression of solutions in achieving the end goals.

In summary, I strongly recommend this book to design and verification engineers who are contemplating, or are currently using formal verification; I certainly learned a lot from it! Ben Cohen, SystemVerilog Assertions specialist

An excellent and comprehensive overview of formal verification. This book is very well organized with a lot of useful tips. The book may be helpful for both inexperienced and experienced engineers.

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